Attorney Docket No: 0553-0404

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)
Osamu NAKAMURA	)
Serial No.: 10/809,118	)
Filed: March 25, 2004	)
For: Semiconductor Device And Manufacturing Method Thereof	)
Examiner: Hoai V. Pham	)
Confirmation No.: 7733	)
Art Unit: 2814	)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ELECTION AND AMENDMENT C

In response to the Restriction Requirement of December 27, 2007, a one month extension of time being submitted herewith, Applicant elects to prosecute Species 1.

Applicant is also amending Claims 1-7 and 12-13 to better claim the invention.

Applicant believes that amended Claims 1-7, 12-13 and 21-25 and previously presented Claims 8-11 (i.e. Claims 1-13 and 21-25) read on the elected species. More specifically, independent Claims 1-3 and 6 all include the feature of "the gate interconnection and the source interconnection intersect in the second region, while Claims 4, 5, 7-13 and 21-25 are dependent thereon. Therefore, Claims 1-13 and 21-25 are the elected claims and should be examined in this application.

Applicant is making this election without disclaimer or prejudice to later filing a divisional

application on the non-elected claims and/or species.

Please enter the following amendment in the above-identified application:

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A semiconductor device comprising:

a gate interconnection; [[and]]

a source interconnection; and

an insulating film,

wherein the gate interconnection and a source interconnection are formed over ~~a substrate~~ a same insulating plane, in a first region, ~~; and~~

wherein [[an]] the insulating film is formed between the gate interconnection and the source interconnection, in a second region, ~~where the gate interconnection and the source interconnection intersect~~

wherein the gate interconnection and the source interconnection do not intersect in the first region, and

wherein the gate interconnection and the source interconnection intersect in the second region.

2. (Currently Amended) A semiconductor device comprising:

a gate interconnection; [[and]]

a source interconnection; and

an island-like insulating film,

wherein the gate interconnection and a source interconnection are formed over ~~a substrate~~ a same insulating plane, in a first region, [[and]]

wherein [[an]] the island-like insulating film is formed between the gate interconnection and the source interconnection, in a second region, ~~where the gate interconnection and the source interconnection intersect~~

wherein the gate interconnection and the source interconnection do not intersect in the first region, and

wherein the gate interconnection and the source interconnection intersect in the second region.

3. (Currently Amended) A semiconductor device comprising:

a gate interconnection; [[and]]

a source interconnection;

an island-like insulating film;

an active layer;

a gate insulating film;

wherein the gate interconnection and a source interconnection are formed over ~~a substrate~~ a same insulating plane, in a first region, ~~; and~~

wherein [[an]] the island-like insulating film is formed between the gate interconnection and the source interconnection, in a second region, ~~where the gate interconnection and the source interconnection intersect;~~

~~wherein the gate interconnection and the source interconnection are formed on a same insulating surface in a region where the gate interconnection and the source interconnection do not intersect~~

wherein the active layer is formed over the insulating plane.

wherein the gate insulating film is formed between the active layer and the gate interconnection, in a third region,

wherein the gate interconnection and the source interconnection do not intersect in the first region,

wherein the gate interconnection and the source interconnection intersect in the second region, and

wherein a thin film transistor is formed in the third region.

4. (Currently Amended) A semiconductor device according to any one of claims 2 and 3,

wherein the island-like insulating layer is formed so as to cover the gate interconnection in a second region, ~~where the gate interconnection and the source interconnection intersect;~~ and

wherein the source interconnection is formed over the island-like insulating layer.

5. (Currently Amended) A semiconductor device according to any one of claims 2 and 3,

wherein the island-like insulating layer is formed so as to cover the source interconnection in a second region, ~~where the gate interconnection and the source interconnection intersect;~~ and

wherein the gate interconnection is formed over the island-like insulating layer.

6. (Currently Amended) A semiconductor device comprising:

a source region; [[and]]

a source interconnection;

an island-like insulating film;

an active layer;

a gate insulating film;

wherein the gate interconnection and a source interconnection are formed over ~~a substrate~~ a same insulating plane, in a first region, ~~; and~~

wherein the island-like insulating film is formed between the gate interconnection and the source interconnection, in a second region,

wherein the active layer is formed over the insulating plane,

wherein the gate insulating film is formed between the active layer and the gate interconnection, in a third region,

wherein the gate interconnection and the source interconnection do not intersect in the first region,

wherein the gate interconnection and the source interconnection intersect in the second region,

wherein a thin film transistor is formed in the third region, and

wherein the ~~source region~~ active layer and the source interconnection is directly connected ~~on a same plane~~.

7. (Currently Amended) A semiconductor device according to claim 6

wherein the ~~source region~~ active layer and the source interconnection are connected without through a contact hole.

8. (Previously presented) A semiconductor device according to any one of claims 1 to 3 wherein at least one of the gate interconnection and the source interconnection is formed by discharging a solution containing metal particles.

9. (Previously presented) A semiconductor device according to any one of claims 1 to 3 wherein at least one of the gate interconnection and the source interconnection is formed by discharging a solution containing metal elements.

10. (Previously presented) A semiconductor device according to claim 1 wherein the insulating film is formed by discharging a solution containing an insulating material.

11. (Previously presented) A semiconductor device according to any one of claims 2 and 3 wherein the island-like insulating layer is formed by discharging a solution containing an insulating material.

12. (Currently Amended) A semiconductor device according to Claims 3 and 6, ~~any one of claims 1 to 3 and 5~~ wherein ~~the semiconductor device includes a thin film transistor using~~ the active layer comprises a microcrystalline semiconductor.

13. (Currently Amended) A semiconductor device according to Claims 3 and 6, ~~any one of claims 1 to 3 and 5~~ wherein ~~the semiconductor device includes a thin film transistor using~~ the active layer comprises an organic semiconductor.

14-20 (Canceled)

21. (Currently Amended) A display device including the semiconductor device according to any one of claims 1 to 3 and [[5]] 6.

22. (Currently Amended) A digital still camera including the semiconductor device according to any one of claims 1 to 3 and [[5]] 6.

23. (Currently Amended) A personal computer including the semiconductor device according to any one of claims 1 to 3 and [[5]] 6.

24. (Currently Amended) A mobile computer including the semiconductor device according to any one of claims 1 to 3 and [[5]] 6.

25. (Currently Amended) An image reproducing system including the semiconductor device according to any one of claims 1 to 3 and [[5]] 6.

REMARKS

Applicant is amending Claims 1-7 and 12-13 to better claim the invention and is amending Claims 21-25 to correct a typographical error in the claims. Therefore, it is respectfully requested that these amendments be entered and allowed.

Information Disclosure Statement

Applicant is also submitting an information disclosure statement (IDS) herewith. It is respectfully requested that this IDS be entered and considered prior to the issuance of any further action on this application.

Conclusion

If any fee should be due for this amendment or election, please charge our deposit account 50/1039.

Favorable consideration is earnestly solicited.

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Respectfully submitted,

/Mark J. Murphy/
Mark J. Murphy
Registration No. 34,225

COOK, ALEX, McFARRON, MANZO,
CUMMINGS & MEHLER, Ltd.
200 West Adams Street, Suite 2850
Chicago, Illinois 60606
(312) 236-8500

Customer No. 26568